PATENT

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TITLE: System and Method for Synchronizing an Asynchronous Frequency for use in a Digital System

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Title: System and Method for Synchronizing an Asynchronous Frequency for use in a Digital System

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Field of the Invention

This invention relates to digitally controlled oscillators, particularly for use in a digital phase-locked loop (PLL), for accurately detecting an asynchronous frequency within a synchronous digital system. More particularly, the invention relates to a method for preconditioning the asynchronous frequency so that it does not introduce additional phase noise at low frequencies within the digital PLL.

Description of the Related Art

Analog-to-digital converters (ADCs) are circuits used to convert signals from the analog domain, where the signals are represented by continuous quantities such as voltage and current, to the digital domain, where the signals are represented by numbers. These circuits can be implemented in a large number of ways. Established A/D conversion techniques include flash, delta-sigma (or sigma-delta), sub-ranging, successive approximation, and integrating.

One example of an A/D converter is an over-sampled A/D converter. Oversampled A/D converters, often denoted as "delta-sigma converters" or "sigma-delta converters" are well known in the art. Delta-sigma (D/S) converters have gained in popularity due primarily to their ability to realize high resolution analog-to-digital conversion in mixed signal VLSI processes.

A D/S converter essentially digitizes an analog signal at a very high sampling rate (oversampling) in order to perform a noise shaping function. Digital filtering after the noise shaping allows the D/S converter to achieve a high resolution when compared with

conventional A/D converters. Decimation is thereafter used to reduce the effective sampling rate back to the "Nyquist" rate.

Oversampled sigma-delta digital-to-analog (D/A) and analog-to-digital (A/D) converters use interpolation and decimation filters, respectively. Such filters typically require a high frequency clock signal that is a binary multiple of either an input sample rate or an output sample rate. In other words, the interpolation filter in the D/A converter requires a high frequency clock signal that is a simple binary multiple of the input sample rate, whereas the A/D converter, using a decimation filter, usually requires a high frequency clock signal that is a simple binary multiple of the output sample rate.

As described in the Background section of U.S. Patent No. 5,638,010, in systems that must accommodate a variety of input sample rates, generating the required high frequency master clock that is a multiple of the input sample rate can be difficult. Frequently, an analog phase-locked loop (PLL) has been required to generate this clock, which limits the ability to use an asynchronous master clock. U.S. Patent No. 5,638,010 notes that it would be preferable to use a digital PLL to provide a single digital integrated circuit which accommodates a number of input sample rates. A digital PLL would eliminate the requirement of an analog PLL and allow a user to provide only an asynchronous master clock instead of a master clock phase-locked to the input rate. U.S. Patent No. 5,638,010 notes that Analog Devices, Inc. has a product called the AD1843 which comprises such a system, although this product disadvantageously uses a complex noise shaping scheme to overcome the problems caused by using a digital PLL.

U.S. Patent No. 5,638,010 describes a method to accurately detect an asynchronous frequency within a synchronous digital system. The asynchronous frequency is synchronized to a master (synchronous) clock and a residue is output. The system uses a digital PLL. An inherent advantage to the described system is that phase noise in the input asynchronous frequency is filtered for frequencies above the PLL system bandwidth. Unfortunately this system also adds phase noise to the input that can not be removed by the digital PLL for frequencies below the system bandwidth.

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More particularly, Figure 1 shows the interface signals to the digital PLL in U.S. Patent No. 5,638,010. The digital PLL receives a high frequency master clock (MASTER CLOCK, 64) an asynchronous low frequency sample clock (44.1 kHz CLOCK, 34). The PLL outputs a CLOCK OUT, 36a, which is a synchronized version of the clock input (44.1 kHz CLOCK, 34). Because of the synchronization, a time difference between the clock input 34 and the clock output 36a is introduced. The PLL also outputs a LATCHED RESIDUE, 77, which is a digital number that attempts to describe the time difference. The time difference contains useful information for an interpolation filter.

The PHASE DETECTOR 80 inherent to the Digital PLL (see Figure 3 of Patent No. 5,638,010) contains a synchronization of the clock input 34. This is described in the text for the patent at column 6, line 3, which states: "In the digital PLL, for the phase detector, if the input signal is asynchronous relative to the master clock, one or more synchronizing latches are normally used to prevent metastability problems."

Because of the synchronization, phase noise is added to the input signal. The digital PLL is to some extent insensitive to this noise because it contains a loop filter 86 that attenuates noise above its cut off frequency. However, noise below the loop filter cut off frequency is not removed.

Therefore, an improved system and method is desired for accurately detecting an asynchronous frequency within a synchronous digital system that does not introduce additional phase noise at low frequencies within the digital PLL.

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Summary of the Invention

One embodiment of the present invention comprises a system and method for accurately detecting an asynchronous frequency within a synchronous digital system. The improved system and method preconditions the asynchronous frequency so that it does not introduce additional phase noise at low frequencies within a digital PLL.

In one embodiment, the system comprises a digitally controlled oscillator, wherein the digitally controlled oscillator comprises a preconditioner and a digital phase locked loop. The preconditioner receives an input clock signal and a master clock signal. The preconditioner outputs a modified clock signal that is synchronized to the master clock signal. The digital phase locked loop is coupled to receive the modified clock signal output from the preconditioner, wherein the digital phase locked loop also receives the master clock signal. The digital phase locked loop outputs an output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal. Due to the operation of the preconditioner, the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal.

The preconditioner preferably has a higher bandwidth than the digital PLL. Thus the preconditioner may operate to noise shape phase noise of the synchronization to higher frequencies. The digital phase locked loop may then operate to remove the phase noise at the higher frequencies.

In one embodiment, the preconditioner comprises a phase detector, a loop filter, a voltage controlled oscillator (VCO), and a latch connected in series. The phase detector has a first input which receives the input clock signal and a second input. The latch has an input coupled to the output of the VCO and an input which receives the master clock signal. The latch includes an output which generates the modified clock signal, wherein the latch synchronizes the modified clock signal to the master clock signal. The latch output is also coupled to the second input of the phase detector to provide the modified clock signal to the phase detector. The preconditioner preferably has a loop gain that operates to attenuate phase noise introduced internally to the preconditioner.

Brief Description of the Drawings

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

Figure 1 illustrates the interface signals to the digital PLL in U.S. Patent No. 5,638,010;

Figure 2 illustrates one embodiment of the invention; and

Figure 3 is a block diagram of the preconditioner of Figure 2.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

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Detailed Description of the Preferred Embodiment

Incorporation by Reference

The following are hereby incorporated by reference as though fully and completely set forth herein:

U.S. Patent No. 5,638,010 titled "Digitally controlled oscillator for a phase-locked loop providing a residue signal for use in continuously variable interpolation and decimation filters" which issued on June 10, 1997 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

Figure 2 - Embodiment of the Invention

Figure 2 illustrates one embodiment of a system for detecting an asynchronous frequency within a synchronous digital system. As shown, the system includes a digital PLL 104 and a preconditioner 102. The preconditioner 102 includes an input which receives a clock signal 34a. The clock signal 34a may be any frequency, but in this embodiment is 44.1 kHz. The preconditioner 102 receives a master clock 64. The preconditioner 102 outputs a modified or conditioned clock signal 34b to the digital PLL 104. The modified clock signal 34b output by the preconditioner 102 is preferably synchronized to the master clock signal 64. The digital PLL 104 also receives the master clock 64. The digital PLL 104 outputs a Clock Out signal 36a and a Latched Residue signal 77. The Clock Out signal 36a is a version of the input clock signal 34a synchronized to the master clock signal 64.

Thus, as shown in Figure 2, the preconditioner 102 is inserted before the clock input 34 signal. The input 34a to the preconditioner may be similar or identical to the clock signal 34 input to the digital PLL in the system described in U.S. Patent No. 5,638,010. The preconditioner 102 includes logic for preconditioning the asynchronous frequency so that it does not introduce additional phase noise at low frequencies within the digital PLL. The preconditioner outputs a clock signal 34b, that does not cause the

digital PLL 104 to introduce additional phase noise to the clock signal.

The system comprising preconditioner 102 and digital PLL 104 receives a high frequency master clock 64 and an asynchronous low frequency sample clock (e.g., 44.1 kHz clock) 34. The preconditioner 102 preconditions the input clock signal 34a and provides a modified clock signal 34b to the digital PLL 104. The digital PLL 104 outputs an output clock signal 36a, which is a synchronized version of the input clock input 34 (e.g., 44.1 kHz). The modified clock signal 34b provided by the preconditioner 102 helps ensure that the digital PLL 104 does not introduce additional phase noise to the clock signal.

Figure 3 – Preconditioner Block Diagram

Figure 3 is a block diagram for the preconditioner. In one embodiment, the preconditioner comprises an analog phase detector 202, an analog loop filter 204, an analog VCO (voltage controlled oscillator) 206 and a latch 208. The phase detector 202 receives the clock input 34a. The phase detector 202 provides an output to the loop filter 204, which in turn provides an output to the VCO 206, which provides an output to the latch 208. The latch 208 receives the master clock 64. The latch 208 outputs the clock output 34b of the preconditioner 102. The clock output 34b of the latch 208 is also fed back to an input of the phase detector 202.

The phase noise introduced internal to the preconditioner 102 is attenuated by the loop gain factor of the loop of the preconditioner 102. This causes the phase noise of the synchronization to be noise shaped in a way that is equivalent to a delta-sigma A/D converter loop. The phase noise of the synchronization is noise-shaped to higher frequencies, where it can be removed by the subsequent digital PLL. For this reason, the preconditioner 102 preferably has a higher bandwidth compared to the digital PLL 104 so that phase noise gets pushed to frequencies higher than the digital PLL bandwidth.

The preconditioner 102 also operates to noise shape the phase noise of the VCO 206, so that phase noise of the VCO 206 is not important. This allows for an inexpensive

VCO 206. In the preferred embodiment the preconditioner loop should be of at least second order in order to avoid idle tones within the loop. The second order loop also preferably has zero phase delay.

The latch 208 serves to synchronize the output of the VCO 206 to the master clock 64 of the digital PLL 104. Because the output 34b of the preconditioner 102 is synchronized to the master clock 64, the subsequent digital PLL 104 does not introduce any additional phase noise.

Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

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